

T-46-23-10

NOTICE

SEE ORDER OF DATA FOR ERRATA INFORMATION



Integrated Device Technology, Inc.

CMOS STATIC RAM
256K (64K x 4-BIT)

ADVANCED
INFORMATION
IDT61298

FEATURES:

- Fast Output Enable (\overline{OE}) pin available for added system flexibility
- High speed (equal access and cycle times)
 - Military: 25/35/45/55 (max.)
 - Commercial: 20/25/35/45ns (max.)
- Low power consumption
 - IDT61298S
 - Active: 400mW (typ.)
 - Standby: 400 μ W (typ.)
 - IDT61298L
 - Active: 350mW (typ.)
 - Standby: 100 μ W (typ.)
- Battery back-up operation
 - 2V data retention (L version only)
- JEDEC standard pinout
- 300 Mil 28-pin DIP, 300 Mil 28-pin SOJ, and 300 Mil 28-pin LCC
- Produced with advanced CEMOS™ technology
- Bidirectional data inputs and outputs
- Inputs/Outputs TTL-compatible
- Three-state outputs
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT61298 is a 262,144-bit high-speed static RAM organized as 64K x 4. It is fabricated using IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective approach for memory intensive applications.

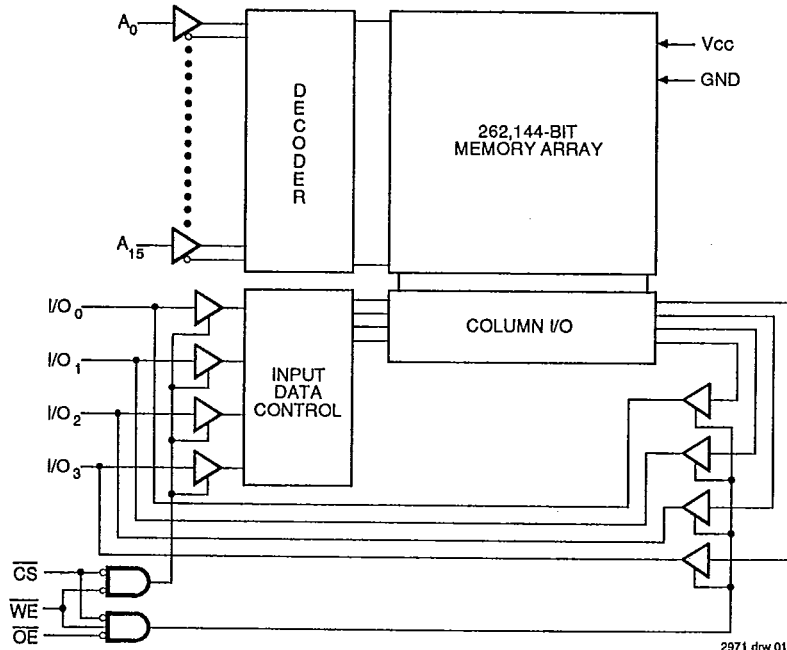
The IDT61298 features two memory control functions: Chip Select (\overline{CS}) and Output Enable (\overline{OE}). These two functions greatly enhance the IDT61298's overall flexibility in high-speed memory applications.

Access times as fast as 20ns are available with typical power consumption of only 350mW. The IDT61298 offers a reduced power standby mode, $ISB1$, which enables the designer to considerably reduce device power requirements. This capability significantly decreases system power and cooling levels, while greatly enhancing system reliability. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 100 μ W when operating from a 2V battery.

All inputs and outputs are TTL-compatible and the device operates from a single 5 volt supply. Fully static asynchronous



FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES

OCTOBER 1990

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IDT61298S/IDT61298L
CMOS STATIC RAM 256K (64K x 4-BIT)

MILITARY AND COMMERCIAL TEMPERATURE RANGES

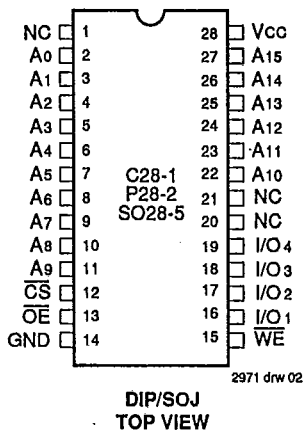
DESCRIPTION (Continued)

circuitry, along with matching access and cycle times, favor the simplified system design approach.

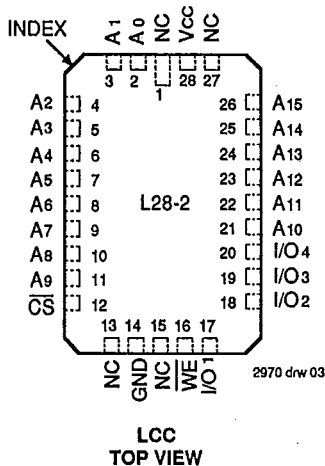
The IDT61298 is packaged in a 28-pin sidebraze or plastic 300mil DIP, an SOJ, plus an LCC, providing improved board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATION



2971 drw 02



2970 drw 03

PIN DESCRIPTIONS

Name	Description
A0-A15	Address Inputs
CS	Chip Select
WE	Write Enable
OE	Output Enable
I/O1-4	Data Input/Output
VCC	Power
GND	Ground

2971 tbl 01

TRUTH TABLE(1)

Mode	CS	WE	OE	I/O	Power
Standby	H	X	X	High Z	Standby
Read	L	H	L	DOUT	Active
Write	L	L	X	DIN	Active
Read	L	H	H	High Z	Active

NOTE:
1. H = V_{IH}, L = V_{IL}, X = Don't Care

2971 tbl 02

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	1.0	1.0	W
IOUT	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2971 tbl 03

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN	Input Capacitance	V _{IN} = 0V	11	pF
COUT	Output Capacitance	V _{OUT} = 0V	11	pF

NOTE:
1. This parameter is determined by device characterization, but is not production tested.

2975 tbl 04

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IDT61298S/IDT61298L
CMOS STATIC RAM 256K (64K x 4-BIT)

MILITARY AND COMMERCIAL TEMPERATURE RANGES

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2971 t05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V _{IH}	Input High Voltage	2.2	—	6.0	V
V _{IL}	Input Low Voltage	-0.5 ⁽¹⁾	—	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

2971 t06

DC ELECTRICAL CHARACTERISTICS⁽¹⁾
(Vcc = 5V ± 10%, V_{LC} = 0.2V, V_{HC} = Vcc - 0.2V)

Symbol	Parameter	Power	61298S20 61298L20		61298S25 61298L25		61298S35 61298L35		61298S45 61298L45		61298S55 61298L55		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I _{CC1}	Operating Power Supply Current CS = V _{IL} , Outputs Open Vcc = Max., f = 0 ⁽²⁾	S	110	—	100	110	100	110	100	110	—	110	mA
		L	100	—	90	100	90	100	90	100	—	100	
I _{CC2}	Dynamic Operating Current CS = V _{IL} , Outputs Open Vcc = Max., f = f _{MAX} ⁽²⁾	S	160	—	150	160	150	160	150	160	—	160	mA
		L	140	—	130	140	130	140	130	140	—	140	
I _{SB}	Standby Power Supply Current (TTL Level) CS ≥ V _{IH} , Vcc = Max., Outputs Open, f = f _{MAX} ⁽²⁾	S	35	—	35	35	35	35	35	35	—	35	mA
		L	20	—	20	20	20	20	20	20	—	20	
I _{SB1}	Full Standby Power Supply Current (CMOS Level) CS ≥ V _{HC} , Vcc = Max., f = 0 ⁽²⁾	S	30	—	30	35	30	35	30	35	—	35	mA
		L	1.5	—	1.5	4.5	1.5	4.5	1.5	4.5	—	4.5	

NOTES:

- All values are maximum guaranteed values.
- At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of 1/trc. f = 0 means no input lines change.

2971 t07



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IDT61298S/DT61298L
CMOS STATIC RAM 256K (64K x 4-BIT)

MILITARY AND COMMERCIAL TEMPERATURE RANGES

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2971 tbl 08

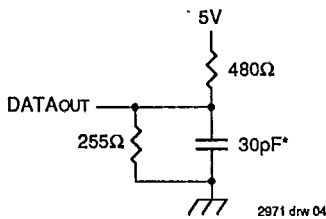


Figure 1. Output Load

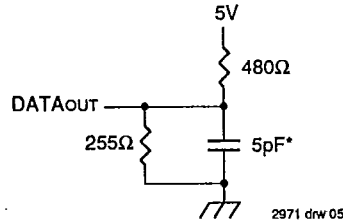


Figure 2. Output Load
(for tCLZ, tOLZ, tCHZ, tOHZ, tLOW, tWHZ)

*Includes scope and jig capacitances

DC ELECTRICAL CHARACTERISTICS

VCC = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT61298S			IDT61298L			Unit	
			Min.	Typ.	Max.	Min.	Typ.	Max.		
I _{LI}	Input Leakage Current	VCC = Max., VIN = GND to VCC	MIL COM'L	—	—	10 5	—	—	5 2	μA
I _{LO}	Output Leakage Current	VCC = Max., CS = VIH, VOUT = GND to VCC	MIL COM'L	—	—	10 5	—	—	5 2	μA
VOL	Output Low Voltage	IOL = 8mA, VCC = Min. IOL = 10mA, VCC = Min.		—	—	0.4 0.5	—	—	0.4 0.5	V
VOH	Output High Voltage	IOH = -4mA, VCC = Min.		2.4	—	—	2.4	—	—	V

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) VHC = VCC - 0.2V

Symbol	Parameter	Test Condition	Min.	Typ. ⁽¹⁾ VCC @		Max. VCC @		Unit
				2.0V	3.0V	2.0V	3.0V	
VDR	VCC for Data Retention	—	2.0	—	—	—	—	V
ICCDR	Data Retention Current		MIL COM'L	—	—	2000 500	3000 750	μA
tCDR ⁽³⁾	Chip Deselect to Data Retention Time	CS ≥ VHC	0	—	—	—	—	ns
tR ⁽³⁾	Operation Recovery Time		tRC ⁽²⁾	—	—	—	—	ns
I _{LI} ⁽³⁾	Input Leakage Current		—	—	—	2	2	μA

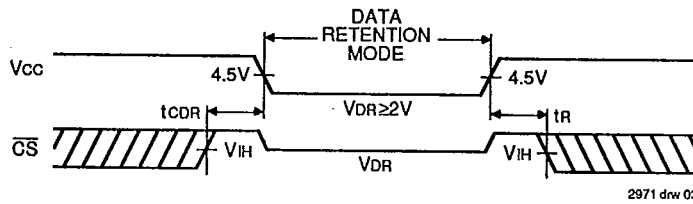
2971 tbl 10

NOTES:

- TA = +25°C.
- tRC = Read Cycle Time.
- This parameter is guaranteed, but not tested.

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LOW V_{CC} DATA RETENTION WAVEFORM



AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	61298S20 ⁽¹⁾ 61298L20 ⁽¹⁾		61298S25 ⁽²⁾ 61298L25 ⁽²⁾		61298S35 61298L35		61298S45 61298L45		61298S55 ⁽²⁾ 61298L55 ⁽²⁾		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
t _{RC}	Read Cycle Time	20	—	25	—	35	—	45	—	55	—	ns
t _{AA}	Address Access Time	—	20	—	25	—	35	—	45	—	55	ns
t _{ACS}	Chip Select Access Time	—	20	—	25	—	35	—	45	—	55	ns
t _{CLZ} ⁽³⁾	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t _{OE}	Output Enable to Output Valid	—	13	—	15	—	25	—	30	—	35	ns
t _{OLZ} ⁽³⁾	Output Enable to Output in Low Z	2	—	3	—	5	—	5	—	5	—	ns
t _{CHZ} ⁽³⁾	Chip Select to Output in High Z	—	10	—	13	—	15	—	20	—	25	ns
t _{OHZ} ⁽³⁾	Output Disable to Output in High Z	—	10	—	13	—	15	—	15	—	20	ns
t _{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
t _{PU} ⁽³⁾	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	ns
t _{PD} ⁽³⁾	Chip Deselect to Power Down Time	—	20	—	25	—	35	—	45	—	55	ns
Write Cycle												
t _{WC}	Write Cycle Time	20	—	20	—	30	—	40	—	50	—	ns
t _{CW}	Chip Select to End of Write	15	—	20	—	30	—	40	—	50	—	ns
t _{AW}	Address Valid to End of Write	15	—	20	—	30	—	40	—	50	—	ns
t _{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
t _{WP}	Write Pulse Width	15	—	20	—	30	—	40	—	50	—	ns
t _{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t _{WHZ} ⁽³⁾	Write Enable to Output in High Z	—	10	—	11	—	15	—	20	—	25	ns
t _{DW}	Data Valid to End of Write	11	—	15	—	20	—	25	—	30	—	ns
t _{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t _{OW} ⁽³⁾	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	ns

- NOTES:
 1. 0° to +70°C temperature range only.
 2. -55°C to +125°C temperature range only.
 3. This parameter guaranteed but not tested.
 4. Preliminary data for military devices only.

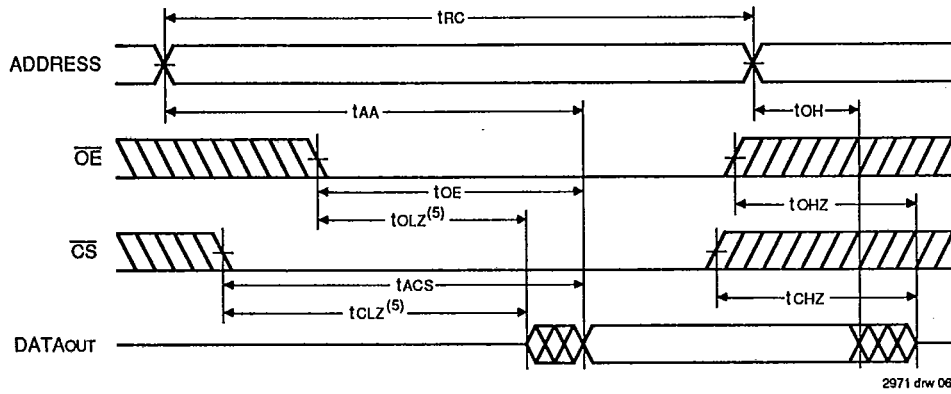
2971 tdt 11

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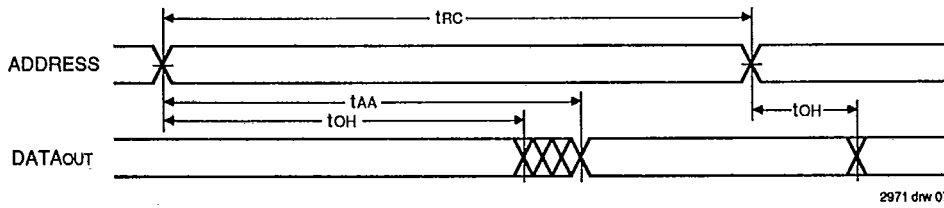
IDT61298S/IDT61298L
CMOS STATIC RAM 256K (64K x 4-BIT)

MILITARY AND COMMERCIAL TEMPERATURE RANGES

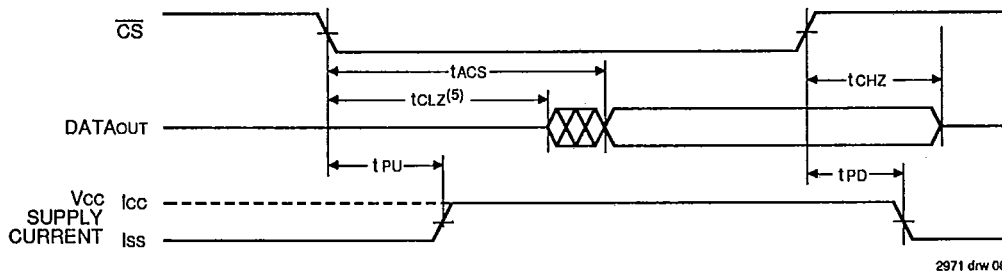
TIMING WAVEFORM OF READ CYCLE NO. 1⁽¹⁾



TIMING WAVEFORM OF READ CYCLE NO. 2^(1,2,4)



TIMING WAVEFORM OF READ CYCLE NO. 3^(1,3,4)



NOTES:

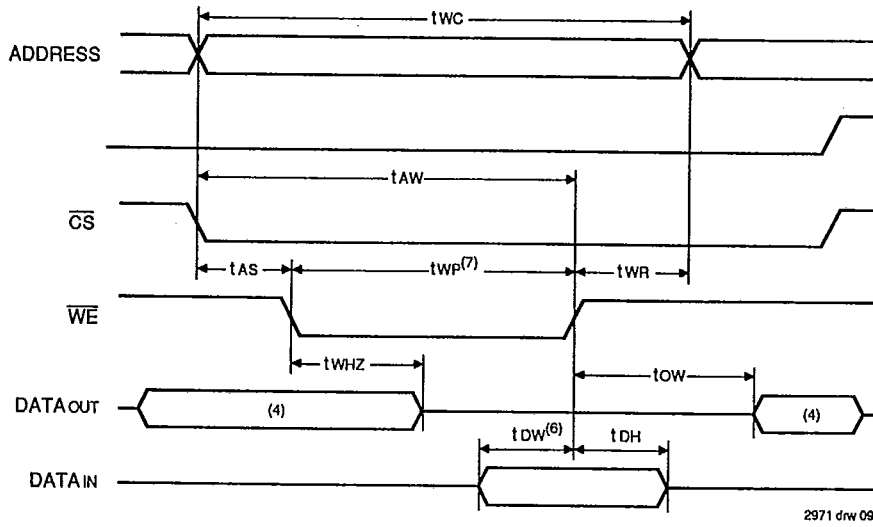
1. WE is high for read cycle.
2. Device is continuously selected, CS = VIL.
3. Address valid prior to or coincident with CS transition low.
4. OE = VIL.
5. Transition is measured ±200mV from steady state.

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IDT61298S/IDT61298L
CMOS STATIC RAM 256K (64K x 4-BIT)

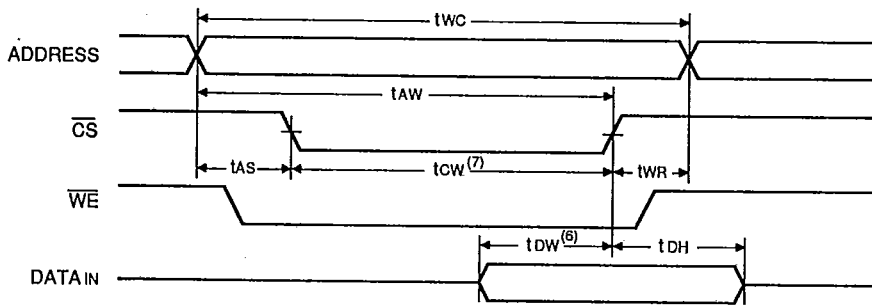
MILITARY AND COMMERCIAL TEMPERATURE RANGES

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (\overline{WE} CONTROLLED TIMING)^(1,2,3,7)



2971 drw 09

TIMING WAVEFORM OF WRITE CYCLE NO. 2 (\overline{CS} CONTROLLED TIMING)^(1,2,3,5)



2971 drw 10

NOTES:

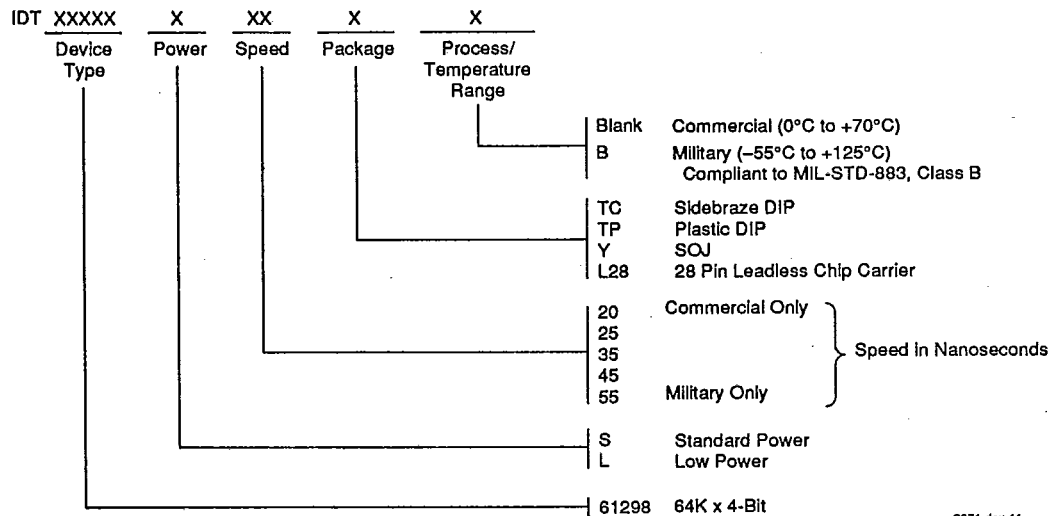
1. \overline{WE} must be high during all address transitions.
2. A write occurs during the overlap (t_{CW} or t_{WP}) of a low \overline{CS} and a low \overline{WE} .
3. t_{WR} is measured from the earlier of \overline{CS} or \overline{WE} going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the \overline{CS} low transition occurs simultaneously with or after the \overline{WE} low transition, the outputs remain in a high impedance state.
6. Transition is measured $\pm 200\text{mV}$ from steady state with a 5pF load (including scope and jig).
7. If \overline{OE} is low during a \overline{WE} controlled write cycle, the write pulse width must be the larger of t_{WP} or $(t_{WHZ} + t_{OW})$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{OW} . If \overline{OE} is high during a \overline{WE} controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP} .

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IDT61298S/IDT61298L
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MILITARY AND COMMERCIAL TEMPERATURE RANGES

ORDERING INFORMATION



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